



荣湃
2PAI SEMICONDUCTOR

3.75kVrms/5.0kVrms Isolated Single Channel Gate Driver

Data Sheet

Pai8211x

FEATURES

Feature options

- Split outputs Pai8211A
- Miller clamp Pai8211C

6A peak source and sink drive current

2.5V to 5.5V input supply voltage

Up to 33V driver supply voltage

8V and 12V UVLO options

3.75kVrms and 5.0kVrms isolation voltage

100kV/us minimum CMTI

51ns typical propagation delay

CMOS inputs

Safety and regulatory approvals:

UL certificate number: UL-US-L494497-11-52017102-10
3.75kVrms/5.0kVrms for 1 minute per UL 1577

VDE certificate number: 40052896
DIN EN IEC 60747-17 (VDE 0884-17):2021-10
 $V_{ORM} = 1200V_{peak}$

CQC certificate number: CQC23001376070
CQC certification per GB 4943.1-2022

AEC-Q100 qualification

Operating temperature range: -40°C to 125°C

RoHS-compliant, NB SOIC-8 and WB SOIC-8 package

APPLICATIONS

Switched-Mode Power Supplies

EV/HEV Inverters and DC/DC Converters

Solar Inverters

Motor Control

UPS and PSU

GENERAL DESCRIPTION

The Pai8211x is a single-channel isolated gate driver family. NB SOIC-8 package and WB SOIC-8 package, can support 3.75kVrms isolation voltage and 5.0kVrms isolation voltage per UL 1577. The Pai8211A provides a split output that controls the rise and fall times individually. The Pai8211C offers an internal clamp function, connecting the gate of the transistor to prevent false turn-on caused by miller current.

The Pai8211x output V_{CC2} operating range from 9.5V to 33V, enables effective driving with Si or SiC MOSFET and IGBT power switches. Integrated UVLO protection ensures output held at low under abnormal conditions. The input V_{CC1} operates from 2.5V to 5.5V, which supports most digital controllers.

Compared to an optocoupler, Pai8211x has lower propagation delay, lower part-to-part skew, higher operating temperature and higher CMTI. It is very convenient to drive MOSFET/IGBT.

Device Information

PART SERIES	UVLO	PIN CONFIGURATION
Pai8211A	8V	Split output
Pai8211C	12V	Miller clamp

FUNCTIONAL BLOCK DIAGRAMS

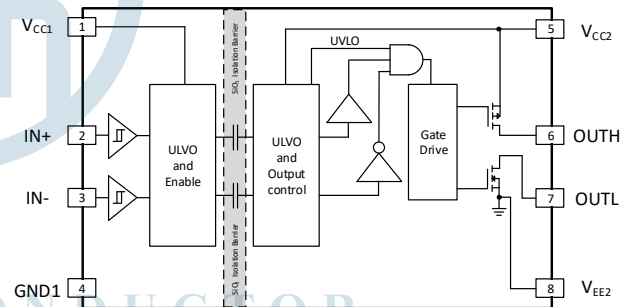


Figure1. Pai8211A Functional Block Diagrams

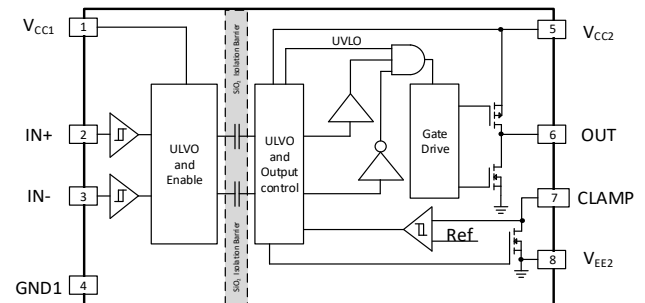


Figure2. Pai8211C Functional Block Diagrams

Rev.1.1

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PIN CONFIGURATIONS AND FUNCTIONS

Table1. Pai8211A Pin Function Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	V _{CC1}	P	Input power supply
2	IN+	I	Positive input
3	IN-	I	Negative input
4	GND1	G	Input ground
5	V _{CC2}	P	Output power supply
6	OUTH	O	Pull high output
7	OUTL	O	Pull low output
8	V _{EE2}	G	Output ground

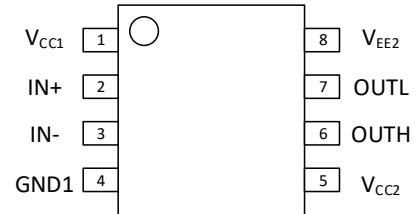


Figure3. Pai8211A Pin Configuration

Table2. Pai8211C Pin Function Descriptions

PIN	NAME	TYPE	DESCRIPTION
1	V _{CC1}	P	Input power supply
2	IN+	I	Positive input
3	IN-	I	Negative input
4	GND1	G	Input ground
5	V _{CC2}	P	Output power supply
6	OUT	O	Gate drive output
7	CLAMP	O	Active miller clamp
8	V _{EE2}	G	Output ground

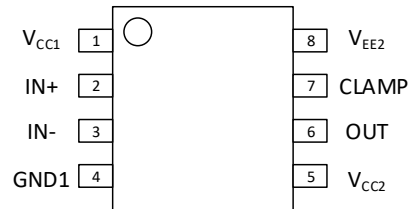


Figure4. Pai8211C Pin Configuration

SPECIFICATIONS

Absolute Maximum Ratings

Table3. Pai8211x Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

DESCRIPTION		MIN	MAX	UNIT
V _{CC1}	Input supply voltage (reference to GND1)	-0.3	7	V
V _{In+} /V _{In-}	Signal input voltage	-0.3	V _{CC1} +0.3	V
V _{CC2}	Output supply voltage (reference to V _{EE2})	-0.3	36	V
Output signal voltage	V _{OUTH} =V _{EE2} , V _{OUTL} =V _{EE2} , V _{OUT} =V _{EE2} , V _{CLAMP} =V _{EE2}	V _{EE2} -0.3	V _{CC2} +0.3	V
T _J	Junction temperature	-40	150	°C
T _{STG}	Storage temperature	-65	150	°C

⁽¹⁾ Operating beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

ESD Rating

Table4. Pai8211x ESD Ratings

DESCRIPTION		Value	UNIT
V _(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	+/-6000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	+/-2000	

⁽¹⁾ JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

⁽²⁾ JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operation Conditions

Table5. Pai8211x Recommended Operating Conditions

DESCRIPTION		MIN	MAX	UNIT
V _{CC1}	Input supply voltage	2.5	5.5	V
V _{In+} /V _{In-}	Input side signal voltage	0	V _{CC1}	V
V _{CC2}	Output supply voltage for Pai8211A	9.5	33	V
V _{CC2}	Output supply voltage for Pai8211C	13.2	33	V

DESCRIPTION		MIN	MAX	UNIT
T _A	Ambient temperature	-40	125	°C

Truth Table

Table6. Pai8211A Truth Table

V _{CC1}	IN+	IN-	V _{CC2}	OUTH	OUTL
above UVLO	L ⁽¹⁾ or floating	X	above UVLO	Hi-Z	L
above UVLO	H	H or floating	above UVLO	Hi-Z	L
above UVLO	H	L	above UVLO	H	Hi-Z
X	X	X	below UVLO	Hi-Z	L
below UVLO	X	X	X	Hi-Z	L

⁽¹⁾ L = Logic Low, H = Logic High, X = H, L or floating, Hi-Z = High impedance.

Table7. Pai8211C Truth Table

V _{CC1}	IN+	IN-	V _{CC2}	OUT	CLAMP
above UVLO	L ⁽¹⁾ or floating	X	above UVLO	L	L
above UVLO	H	H or floating	above UVLO	L	L
above UVLO	H	L	above UVLO	H	Hi-Z
X	X	X	below UVLO	L	L
below UVLO	X	X	X	L	L

⁽¹⁾ L = Logic Low, H = Logic High, X = H, L or floating, Hi-Z = High impedance.

Thermal Information

Table8. Pai8211x Thermal Information

PACKAGE THERMAL RATINGS	NB SOIC-8	WB SOIC-8	UNIT
R _{θJA} Junction-to-ambient thermal resistance	110	100	°C/W
ψ _{JT} Junction-to-top characterization parameter	18	16	°C/W

Supply Power Ratings

Table9. Pai8211x-SR NB SOIC-8 Package Supply Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _D Maximum power dissipation on input and output	V _{CC1} = 5V, V _{CC2} = 15V, f = 1.8MHz, 50% duty cycle, square wave, 2.2nF load			1.14	W
P _{D1} Maximum input power dissipation				0.01	W
P _{D2} Maximum output power dissipation				1.13	W

Table10. Pai8211x-W5R WB SOIC-8 Package Supply Power Ratings

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
P _D Maximum power dissipation on input and output	V _{CC1} = 5V, V _{CC2} = 15V, f = 2.0MHz, 50% duty cycle, square wave, 2.2nF load			1.26	W
P _{D1} Maximum input power dissipation				0.01	W
P _{D2} Maximum output power dissipation				1.25	W

Electrical Specifications

Table11. Pai8211x Electrical Specifications

V_{CC1} = 2.5V or 3.3V or 5V, 0.1uF capacitor from V_{CC1} to GND1, V_{CC2} = 15V, 1uF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1nF. T_A = -40°C to 125°C (Unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS					
I _{VCC1} V _{CC1} quiescent current	V _{IN-} = 0V, V _{IN+} = 0V		0.8	1.2	mA
I _{VCC2} V _{CC2} quiescent current	V _{IN-} = 0V, V _{IN+} = 0V		1.8	2.7	mA
SUPPLY VOLTAGE UNDER VOLTAGE THRESHOLDS					
V _{UV+(VCC1)}	V _{VCC1} under voltage rising threshold	2.10	2.25	2.40	V
V _{UV-(VCC1)}	V _{VCC1} under voltage falling threshold	2.00	2.10	2.20	V
V _{HYS(VCC1)}	V _{VCC1} UVLO threshold hysteresis	0.10	0.15		V
Pai8211A DRIVER SUPPLY VOLTAGE UNDER VOLTAGE THRESHOLDS					
V _{UV+(VCC2)}	V _{VCC2} under voltage rising threshold		8.4	9.4	V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UV-(VCC2)}$	V_{VCC2} under voltage falling threshold	7.1	7.8		V
$V_{HYS(VCC2)}$	V_{VCC2} UVLO threshold hysteresis		0.6		V
Pai8211C DRIVER SUPPLY VOLTAGE UNDER VOLTAGE THRESHOLDS					
$V_{UV+(VCC2)}$	V_{VCC2} under voltage rising threshold		12	13	V
$V_{UV-(VCC2)}$	V_{VCC2} under voltage falling threshold	9.8	10.8		V
$V_{HYS(VCC2)}$	V_{VCC2} UVLO threshold hysteresis		1.2		V
INPUT					
V_{INH}	Input rising threshold		$0.50 \cdot V_{CC1}$	$0.60 \cdot V_{CC1}$	V
V_{INL}	Input falling threshold	$0.30 \cdot V_{CC1}$	$0.35 \cdot V_{CC1}$		V
V_{HYS}			$0.15 \cdot V_{CC1}$		
OUTPUTS (Pai8211A ONLY)					
I_{OH}/I_{OL}	Peak source and sink current $C_{LOAD} = 0.22\mu F$, without external current limiting resistors, 1kHz switching frequency	6	10		A
V_{OH}	High-level output voltage ($V_{CC2} - V_{OUTH}$) $I_{OUTH} = -20mA$		100	150	mV
V_{OL}	Low-level output voltage ($V_{OUTL} - V_{EE2}$) $I_{OUTL} = 20mA$		7.5	11.5	mV
OUTPUTS (Pai8211C ONLY)					
I_{OUT}	Peak source current $C_{LOAD} = 0.22\mu F$, without external current limiting resistors, 1kHz switching frequency	6	10		A
V_{OUTH}	High-level output voltage ($V_{CC2} - V_{OUT}$) $I_{OUT} = -20mA$		100	150	mV
V_{OUTL}	Low-level output voltage ($V_{OUT} - V_{EE2}$) $I_{OUT} = 20mA$		7.5	11.5	mV
ACTIVE MILLER CLAMP (Pai8211C ONLY)					
V_{CLAMP}	Low level clamp voltage $I_{CLAMP} = 20mA$		7	10	mV
I_{CLAMP}	Clamp low level current $V_{CLAMP} = V_{EE2} + 15V$	6	10		A
$V_{CLAMP-TH}$	Clamp threshold voltage $IN+ = \text{high}, IN- = \text{low}$		2.1	2.3	V
SHORT CIRCUIT CLAMPING (Pai8211C ONLY)					
$V_{CLP-OUT}$	Clamping voltage ($V_{OUT} - V_{CC2}$) $IN+ = \text{high}, IN- = \text{low}, t_{CLAMP} = 10\mu s$, $I_{OUT} = 500mA$		1.0	1.3	V
$V_{CLP-OUT}$	Clamping voltage ($V_{EE2} - V_{CLAMP}$) $IN+ = \text{low}, IN- = \text{high},$ $I_{CLAMP} = -20mA$		0.9	1.0	V
ACTIVE PULLDOWN (Pai8211C ONLY)					
V_{OUTSD}	Active pulldown voltage on CLAMP $I_{OUT} = 0.1 \times I_{OUTL(typ)}, V_{CC2} = \text{open}$		1.8	2.5	V
TIMING					
t_{PLH}	Propagation delay, high ⁽¹⁾ $C_{LOAD} = 1.8nF$		51	65	ns
t_{PHL}	Propagation delay, low ⁽¹⁾ $C_{LOAD} = 1.8nF$		51	65	ns
t_{PWD}	Pulse width distortion $C_{LOAD} = 1.8nF$		1	10	ns
t_r	Rise time ⁽²⁾ $C_{LOAD} = 1.8nF$		8	15	ns
t_f	Fall time ⁽²⁾ $C_{LOAD} = 1.8nF$		7	12	ns
CMTI	Common-mode transient immunity ⁽³⁾	100			kV/us

⁽¹⁾ t_{PLH} = low-to-high propagation delay time, t_{PHL} = high-to-low propagation delay time. See Figure22.

⁽²⁾ t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal. See Figure21.

⁽³⁾ See Figure28 for Common-mode transient immunity (CMTI) measurement.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Insulation Specifications

Table12. Pai8211x Insulation Specifications

PARAMETER	SYMBOL	VALUE		UNIT	TEST CONDITIONS/COMMENTS
		NB SOIC-8	WB SOIC-8		
Rated dielectric insulation voltage		3750	5000	Vrms	1-minute duration
Minimum external air gap (Clearance)	L (CLR)	≥4	≥8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum external tracking (Creepage)	L (CRP)	≥4	≥8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum internal gap (Internal clearance)		≥21	≥21	μm	Insulation distance through insulation
Tracking resistance (Comparative tracking index)	CTI	>400	>400	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material group		II	II		According to IEC 60664-1

Package Specifications

Table13. Pai8211x Package Specifications

PARAMETER	SYMBOL	TYPICAL VALUE	UNIT	TEST CONDITIONS/COMMENTS
Resistance (Input to Output) ⁽¹⁾	R _{I-O}	>10 ¹²	Ω	T _A = 25°C
Capacitance (Input to Output) ⁽¹⁾	C _{I-O}	1.5	pF	@ 1MHz
Input Capacitance ⁽²⁾	C _I	3	pF	@ 1MHz

⁽¹⁾ The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4 are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8 are shorted together as the other terminal.

⁽²⁾ Testing from the input signal pin to ground.

Regulatory Information

Table14. Pai8211x Regulatory Information

The insulation lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Regulatory	Pai8211x-SR (NB SOIC-8 Package)	Pai8211x-W5R (WB SOIC-8 Package)
UL	Recognized under UL 1577 component recognition program ⁽¹⁾ single protection, 3750Vrms isolation voltage File number: UL-US-L494497-11-52017102-10	Recognized under UL 1577 component recognition program ⁽¹⁾ single protection, 5000Vrms isolation voltage File number: UL-US-L494497-11-52017102-10
VDE	DIN EN IEC 60747-17 (VDE 0884-17):2021-10 ⁽²⁾ basic insulation, V _{IORM} = 1200Vpeak, V _{IOSM} = 5000Vpeak File number: 40052896	DIN EN IEC 60747-17 (VDE 0884-17):2021-10 ⁽²⁾ basic insulation, V _{IORM} = 1200Vpeak, V _{IOSM} = 5000Vpeak File number: 40052896
CQC	Certified under GB4943.1-2022 Basic insulation at 557Vrms (787Vpeak) working voltage File number: CQC23001376070	Certified under GB4943.1-2022 Basic insulation at 1118Vrms (1580Vpeak) working voltage reinforced insulation at 557Vrms (787Vpeak) File number: CQC23001376070

⁽¹⁾ In accordance with UL 1577, each Pai8211x-SR is proof tested by applying an insulation test voltage ≥ 4500Vrms for 1 sec; each Pai8211x-W5R is proof tested by applying an insulation test voltage ≥ 6000Vrms for 1 sec.

⁽²⁾ In accordance with VDE 0884-17, each Pai8211x is proof tested by applying an insulation test voltage ≥ 1800Vpeak for 1 sec (partial discharge detection limit = 5 pC).

VDE Insulation Characteristics

Table15. VDE Insulation Characteristics

DESCRIPTION	TEST CONDITIONS/COMMENTS	SYMBOL	CHARACTERISTIC		Unit
			Pai8211x-SR NB SOIC-8	Pai8211x-W5R WB SOIC-8	
Overvoltage category per IEC 60664-1	For rated mains voltage $\leq 150\text{Vrms}$ For rated mains voltage $\leq 300\text{Vrms}$ For rated mains voltage $\leq 600\text{Vrms}$ For rated mains voltage $\leq 1000\text{Vrms}$		I to IV I to III NA NA	I to IV I to III I to II	
Climatic category			40/125/21	40/125/21	
Pollution degree			2	2	
Maximum repetitive peak isolation voltage		V_{IORM}	1200	1200	Vpeak
Input to output test voltage, method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1\text{sec}$, partial discharge $< 5\text{pC}$	$V_{pd(m)}$	1800	1800	Vpeak
Input to output test voltage, method A After environmental tests subgroup 1 After input and/or safety test subgroup 2 and subgroup 3	$V_{IORM} \times 1.3 = V_{pd(m)}$, $t_{ini} = 60\text{sec}$, $t_m = 10\text{sec}$, partial discharge $< 5\text{pC}$	$V_{pd(m)}$	1560	1560	Vpeak
	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60\text{sec}$, $t_m = 10\text{sec}$, partial discharge $< 5\text{pC}$		1440	1440	Vpeak
Highest allowable overvoltage		V_{IOTM}	5300	7071	Vpeak
Surge isolation voltage basic	Basic insulation, 1.2/50 μs combination wave, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification) ⁽¹⁾	V_{IOSM}	5000	5000	Vpeak
Safety limiting values	Maximum value allowed in the event of a failure (see Figure6)				
Maximum safety temperature		T_S	150	150	$^{\circ}\text{C}$
Maximum power dissipation at 25 $^{\circ}\text{C}$		P_S	1.14	1.26	W
Insulation resistance	$V_{IO} = 500\text{V}$ at $T_A = 25^{\circ}\text{C}$	R_{IO}	$>10^{12}$	$>10^{12}$	Ω
	$V_{IO} = 500\text{V}$ at $100^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
	$V_{IO} = 500\text{V}$ at $T_S = 150^{\circ}\text{C}$	R_{IO}	$>10^9$	$>10^9$	Ω

⁽¹⁾ In accordance with VDE 0884-17, Pai8211x is proof tested by applying a surge isolation voltage 6500V.

TYPICAL CHARACTERISTIC

$V_{CC1} = 2.5\text{V}$ or 3.3V or 5V , $0.1\mu\text{F}$ capacitor from V_{CC1} to GND1 , $V_{CC2} = 15\text{V}$, $1\mu\text{F}$ capacitor from V_{CC2} to V_{EE2} , $C_{LOAD} = 1\text{nF}$. $T_A = -40^{\circ}\text{C}$ to 125°C (Unless otherwise noted).

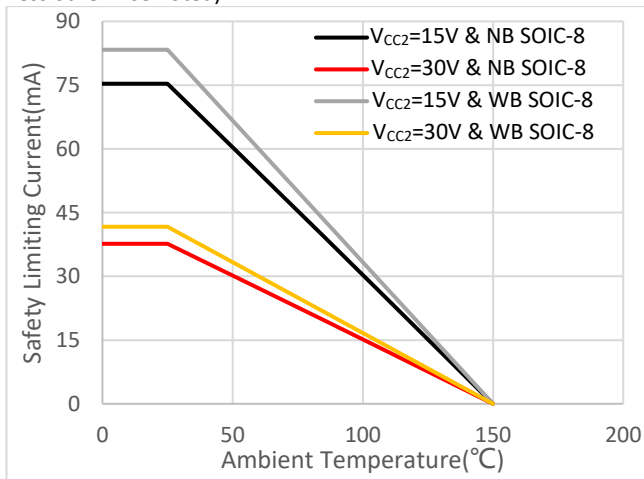


Figure5. NB/WB SOIC-8 Thermal Derating Curve For Limiting Current With Ambient Temperature Per VDE

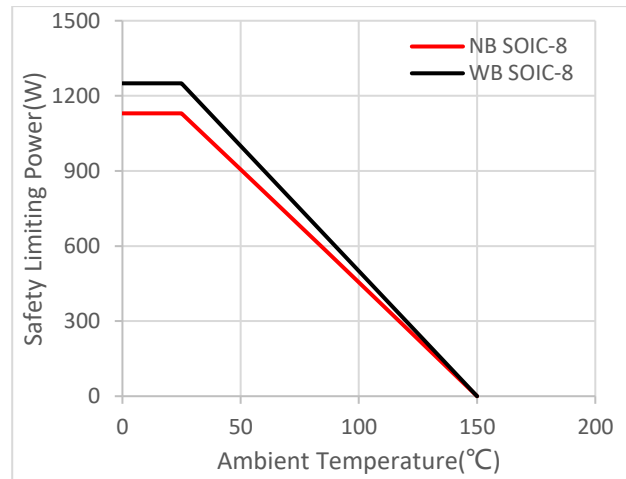
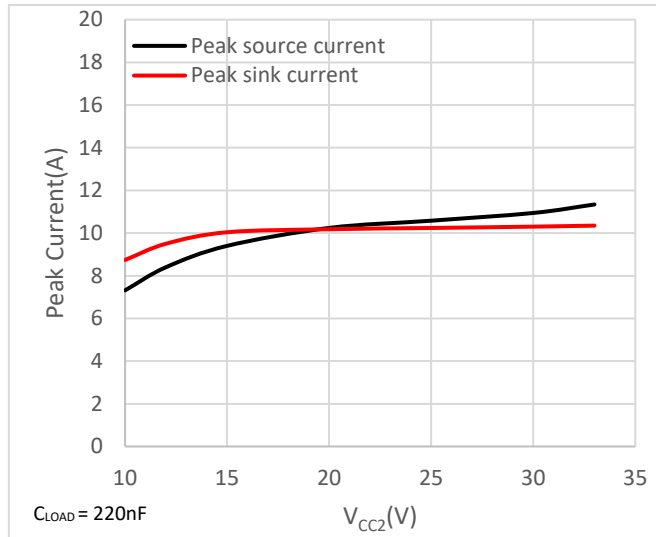
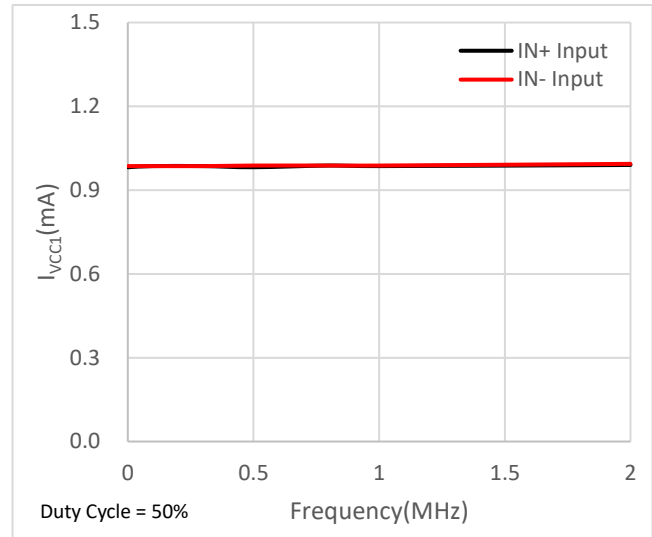
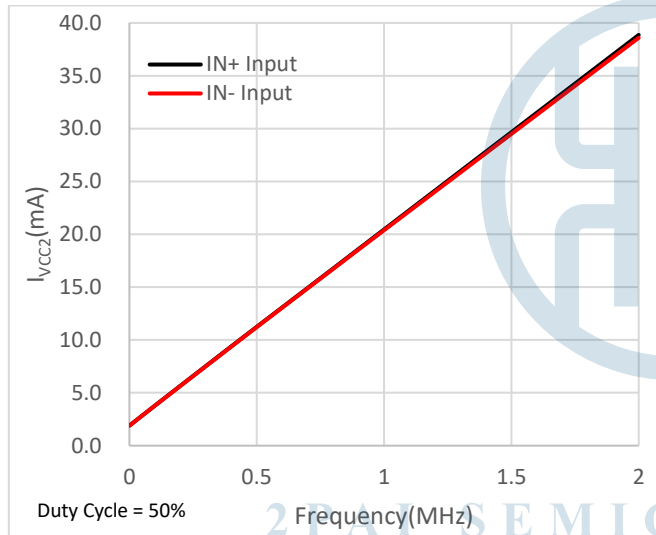
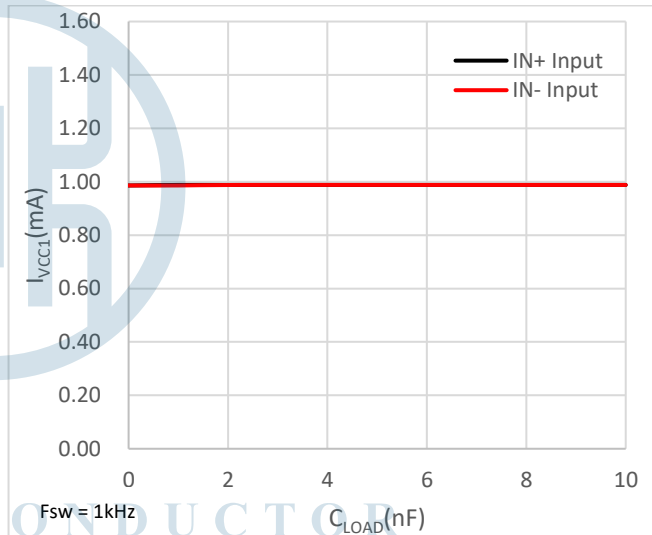
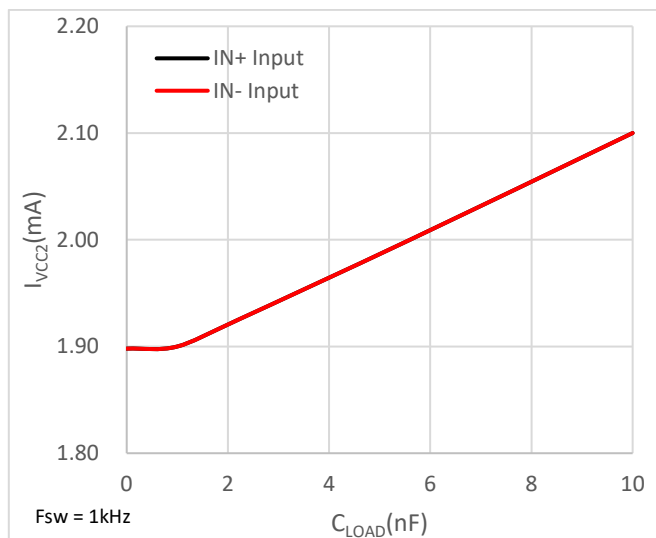
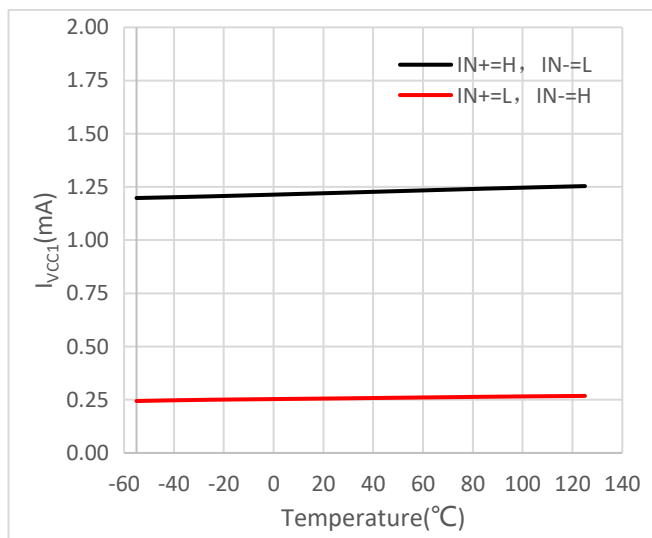


Figure6. NB/WB SOIC-8 Thermal Derating Curve For Limiting Power With Ambient Temperature Per VDE

Figure7. Output High Drive Current Vs V_{CC2} Figure8. I_{VCC1} Supply Current Vs Input FrequencyFigure9. I_{VCC2} Supply Current Vs Input FrequencyFigure10. I_{VCC1} Supply Current Vs Load CapacitanceFigure11. I_{VCC2} Supply Current Vs Load CapacitanceFigure12. I_{VCC1} Supply Current Vs Ambient Temperature

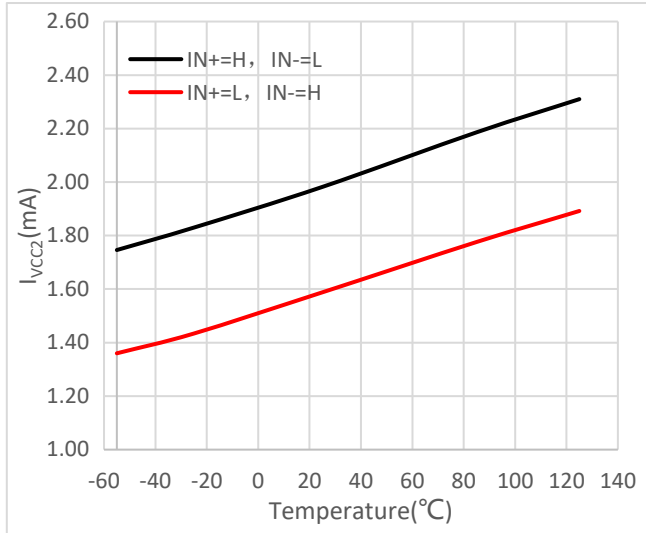
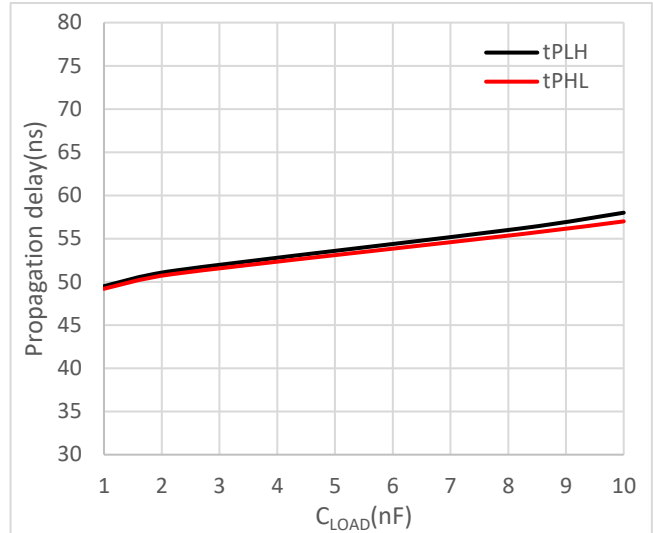
Figure13. I_{VCC2} Supply Current Vs Ambient Temperature

Figure14. Propagation Delay Vs Load Capacitance

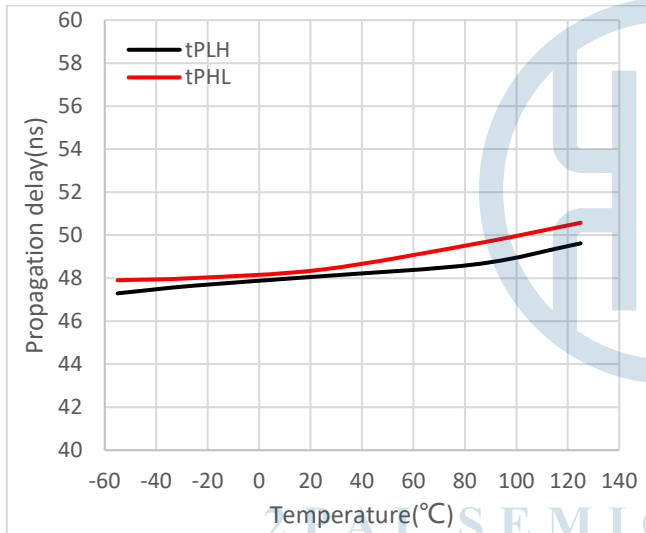


Figure15. Propagation Delay Vs Ambient Temperature

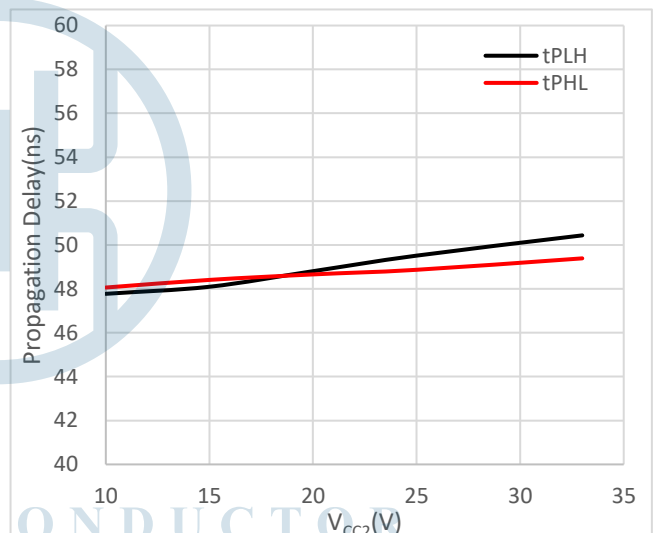
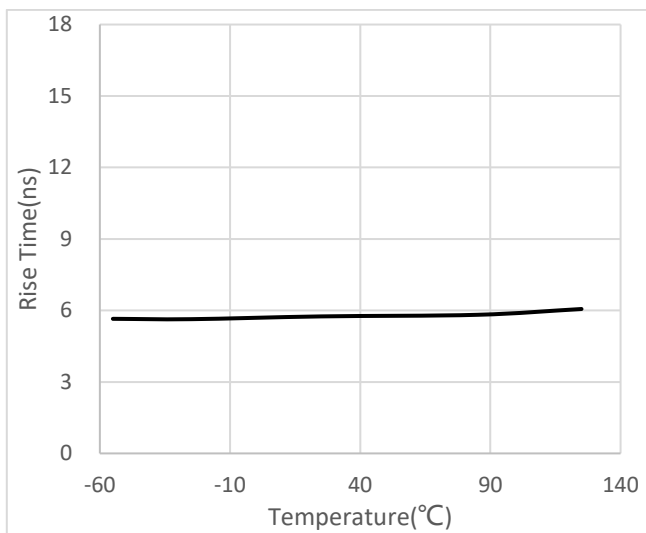
Figure16. Propagation Delay Vs V_{CC2} 

Figure17. Rise Time Vs Ambient Temperature

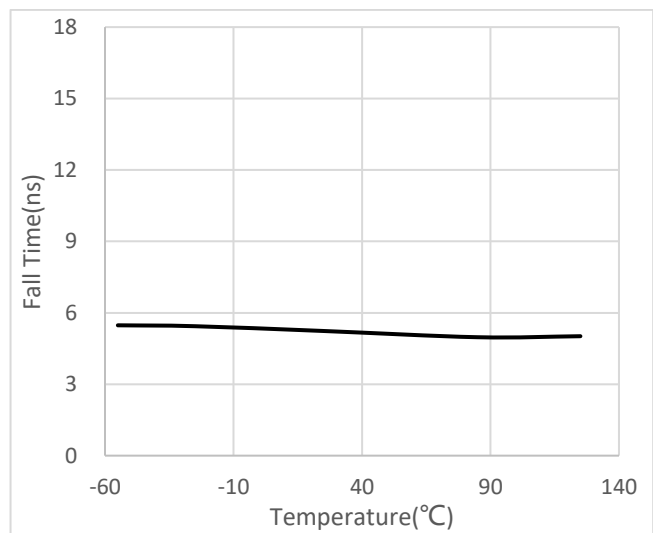
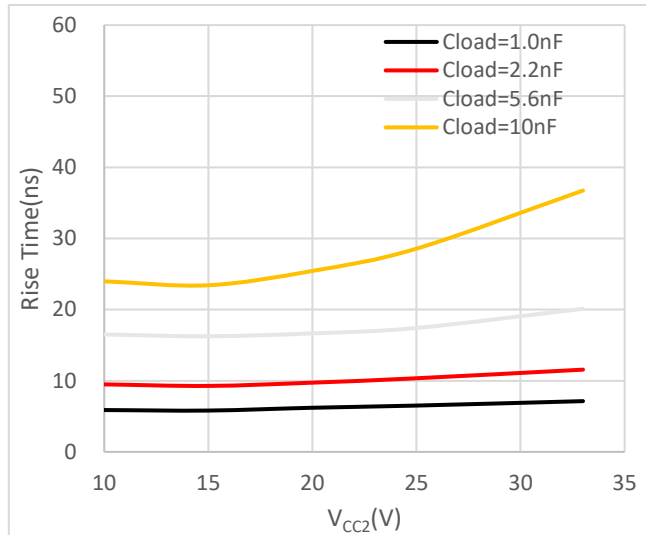
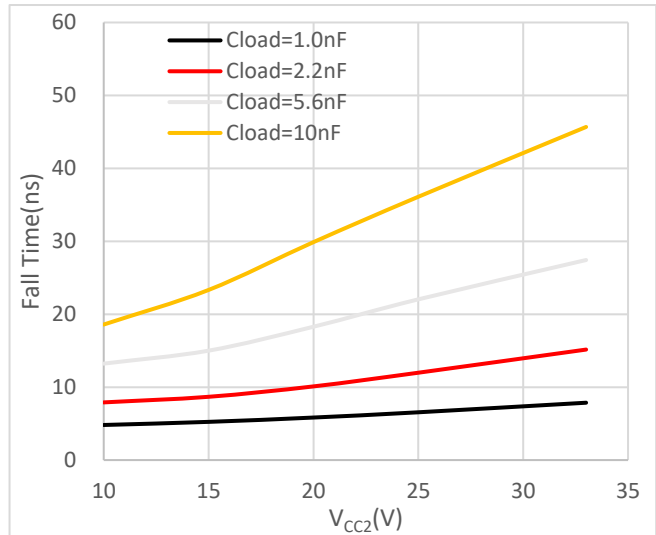


Figure18. Fall Time Vs Ambient Temperature

Figure19. Rise Time Vs C_{LOAD} And V_{CC2} Figure20. Fall Time Vs C_{LOAD} And V_{CC2}

TIMING TEST INFORMATION

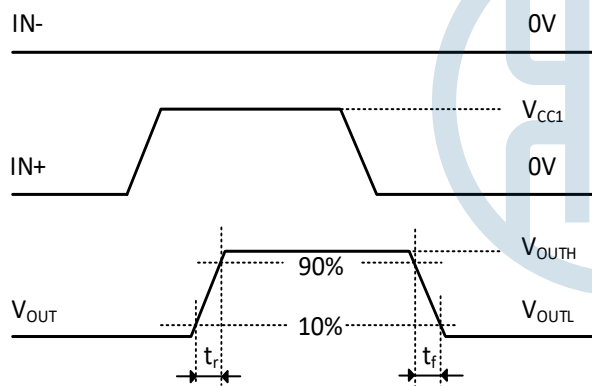


Figure21. Transition Time Waveform Measurement

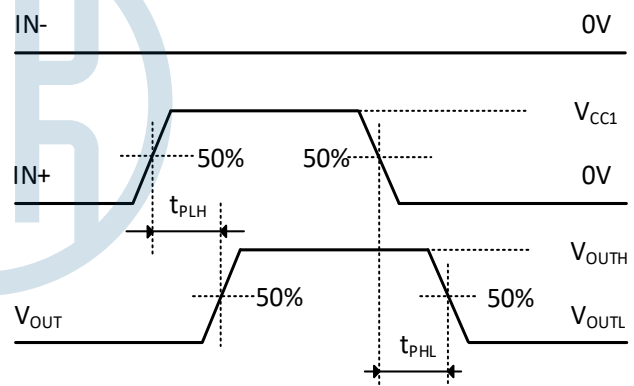


Figure22. Propagation Delay Time Waveform Measurement

APPLICATIONS INFORMATION

Typical Application

The circuit figure below is a typical application for driving IGBTs.

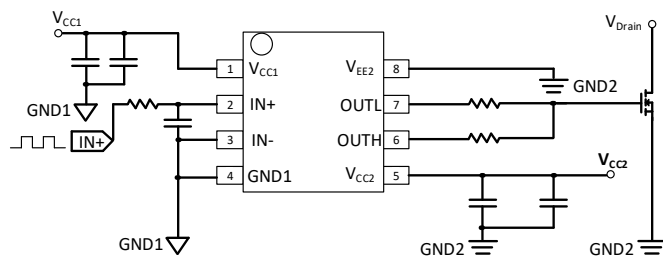


Figure 23. Pai8211A Typical Application Circuit (IN+ Input)

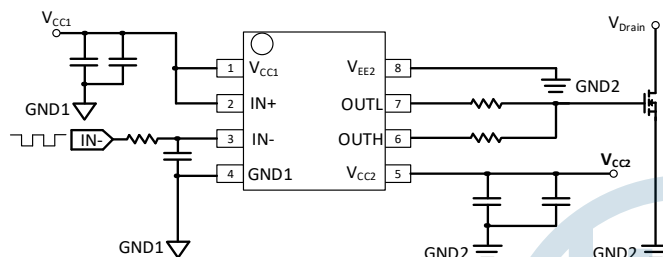


Figure 24. Pai8211A Typical Application Circuit (IN- Input)

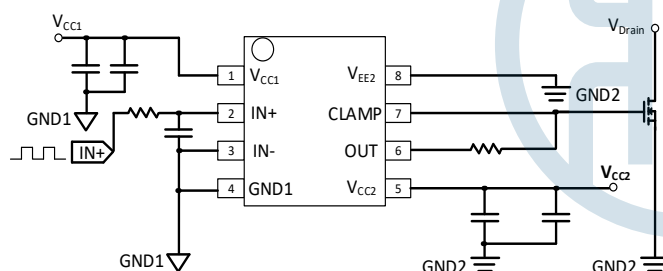


Figure 25. Pai8211C Typical Application Circuit (IN+ Input)

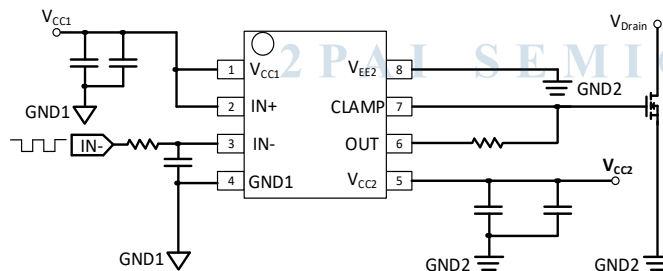


Figure 26. Pai8211C Typical Application Circuit (IN- Input)

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{CC1} and GND1 and between V_{CC2} and V_{EE2} . The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value between V_{CC1} and GND1 is between 0.1 μ F and 1 μ F, bypass capacitor value between V_{CC2} and V_{EE2} is between 1 μ F and 10 μ F. Additional 100nF capacitor in parallel with the isolator device bypass capacitor is recommended for high frequency filtering.

To avoid large negative transients on the V_{EE2} pins connected to the switch node, the parasitic inductances between the source of

the top transistor and the source of the bottom transistor must be minimized.

Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To avoid reducing the isolation capability, keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

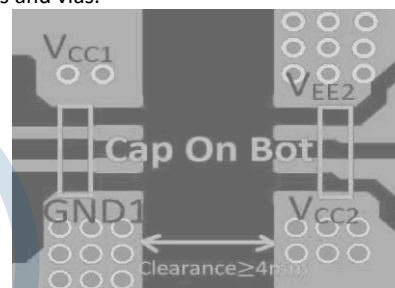


Figure 27. Layout Example

MILLER CLAMP (Pai8211C ONLY)

The active Miller-clamp function is used to prevent false turn-on of the power switches caused by Miller current with applications where a unipolar power supply is used. Low impedance path between the power-switch gate terminal and Miller clamp pins to sink the Miller current is available for the active Miller-clamp function implemented. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2V during the off state.

The Pai8211C provides short-circuit clamping function to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the V_{CC2} voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the V_{CC2} pin inside the driver. The internal diodes can conduct up to 500mA current for a duration of 10 μ s, and a continuous current of 20mA. To improve current conduction capability can use external schottky diodes if needed.

The active pulldown function is used to pull the IGBT or MOSFET gate to the low state, when no power is connected to the V_{CC2} supply. This feature prevents IGBT and MOSFET false turn-on on the OUT and CLAMP pins by clamping the output voltage to approximately 2V.

Figure 25 and Figure 26 show a typical application circuit of Pai8211C.

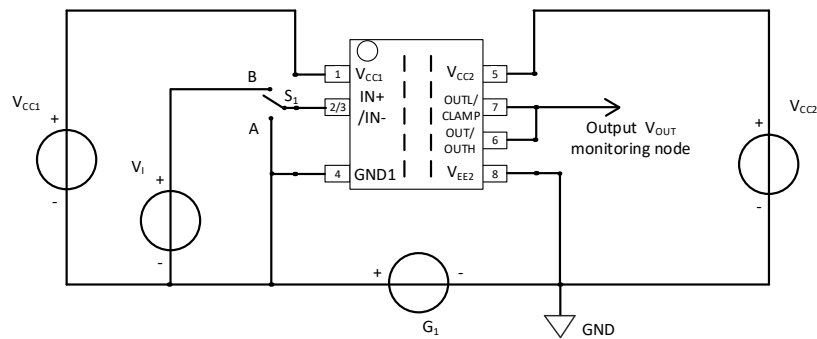
CMTI MEASUREMENT

Figure28. Common-mode Transient Immunity (CMTI) Measurement

Common-Mode Transient Immunity (CMTI) can be measured, under specified common-mode pulse magnitude (VCM), and specified slew rate of the common-mode pulse (dVCM/dt). The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM), such that the maximum common-mode slew rates (dVCM/dt) can be applied to Pai8211x isolator coupler under measurement. The common-mode pulse is applied between one side ground $GND1$ and the other side ground V_{EE2} of Pai8211x isolated gate driver, with positive transients as well as negative transients.



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OUTLINE DIMENSIONS

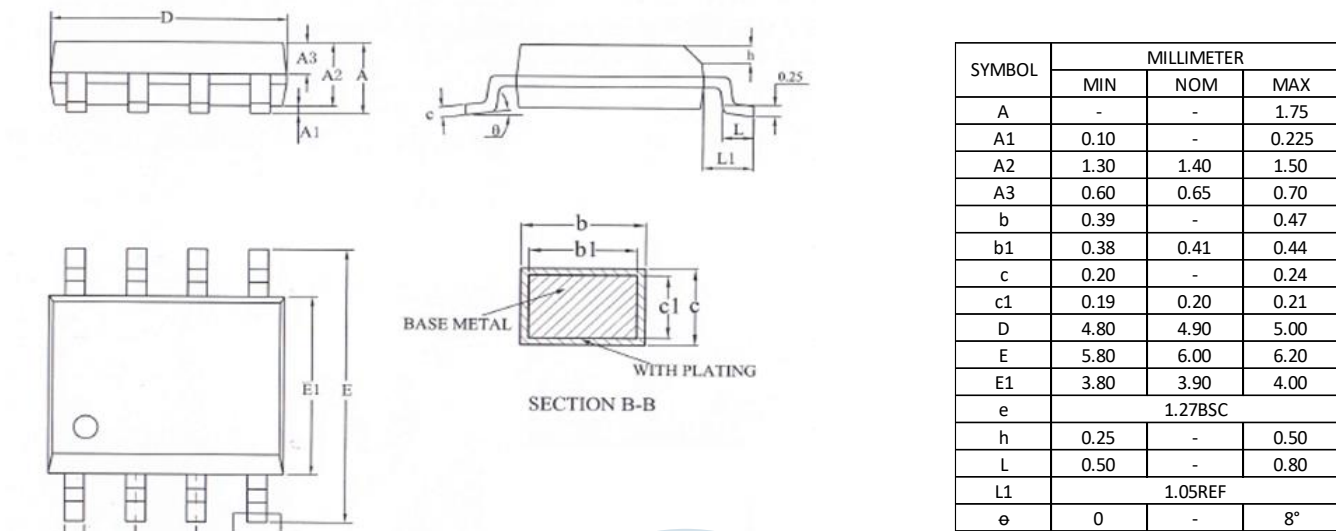


Figure29. 8-Lead Narrow Body SOIC [NB SOIC-8] Outline Package-Dimension Unit(mm)

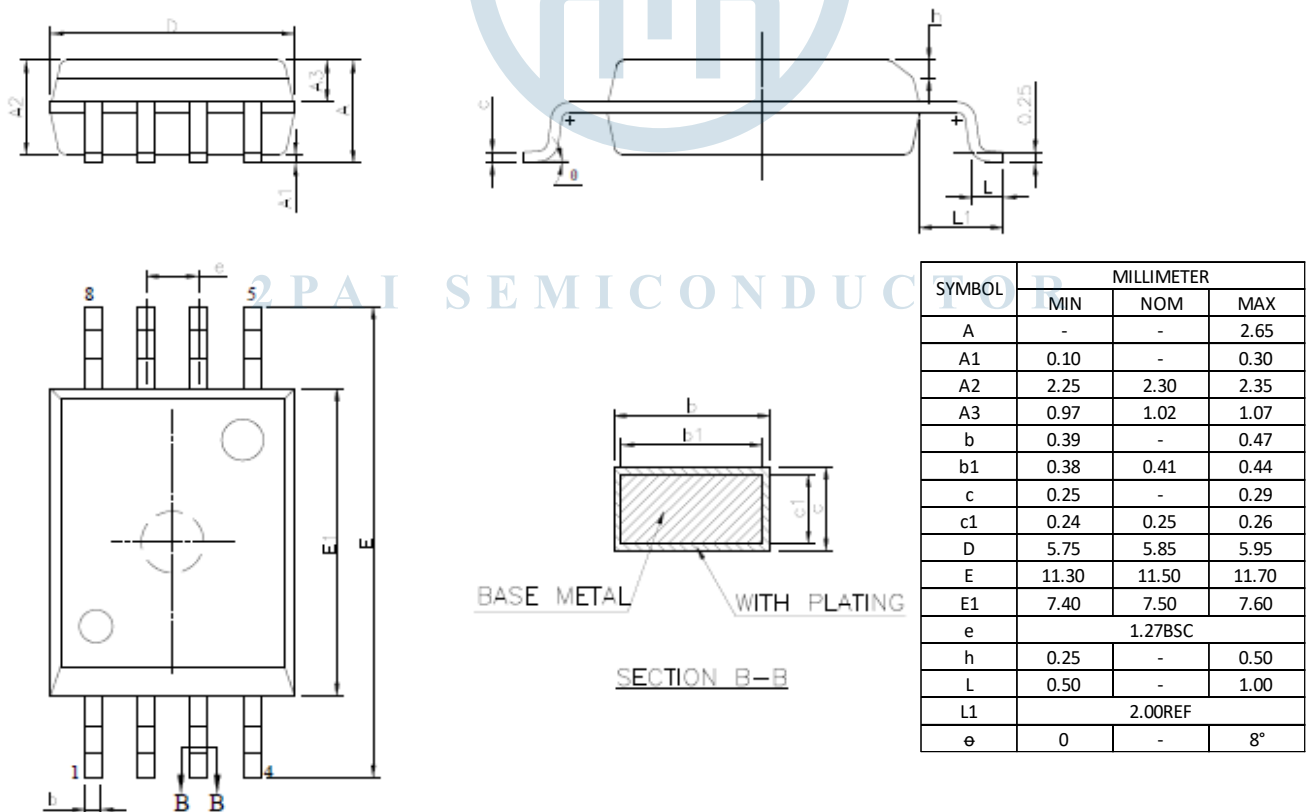


Figure30. 8-Lead Wide Body SOIC [WB SOIC-8] Outline Package-Dimension Unit(mm)

LAND PATTERNS

8-Lead Narrow Body SOIC [NB SOIC-8]

Figure31 illustrates the recommended land pattern details for the Pai82xx in an 8-pin narrow-body SOIC. Table16 lists the values for the dimensions shown in the illustration.

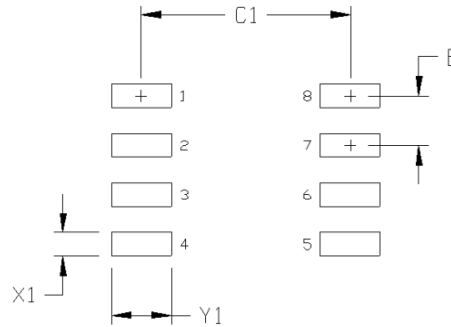


Figure31. 8-Lead Narrow Body SOIC [NB SOIC-8] Land Pattern

Table16. NB SOIC-8 Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

⁽¹⁾ This land pattern design is based on IPC -7351.

⁽²⁾ All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

8-Lead Wide Body SOIC [WB SOIC-8]

Figure32 illustrates the recommended land pattern details for the Pai1xxxxx in an 8-pin narrow-body SOIC. Table17 lists the values for the dimensions shown in the illustration.

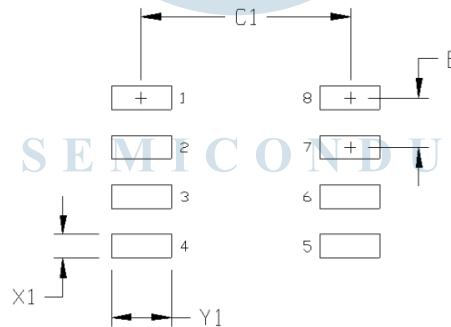


Figure32. 8-Lead Wide Body SOIC [WB SOIC-8] Land Pattern

Table17. WB SOIC-8 Land Pattern Dimensions

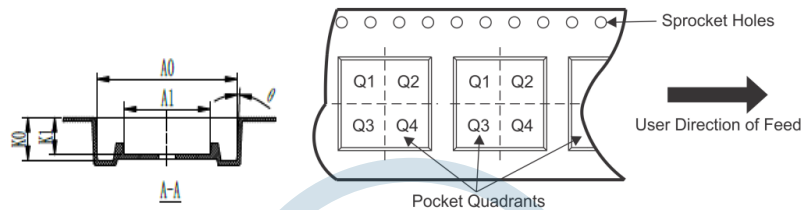
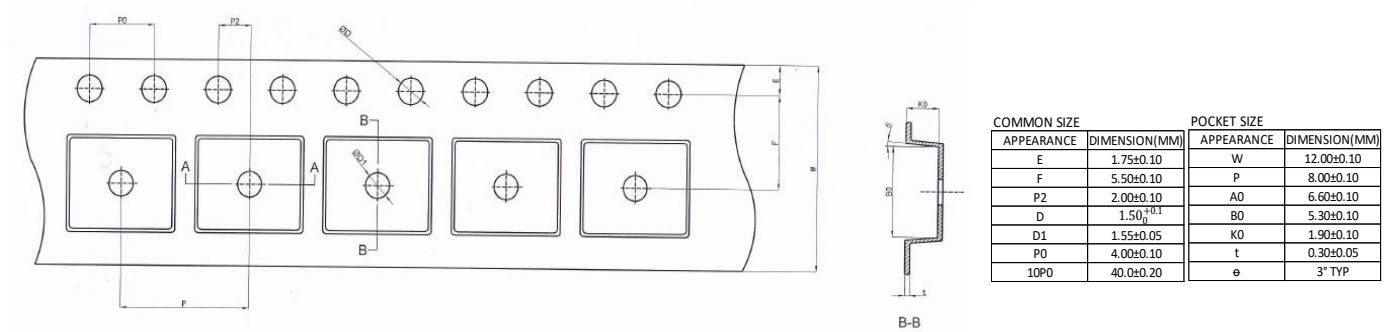
Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.75	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	2.00	mm

⁽¹⁾ This land pattern design is based on IPC -7351.

⁽²⁾ All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

REEL INFORMATION

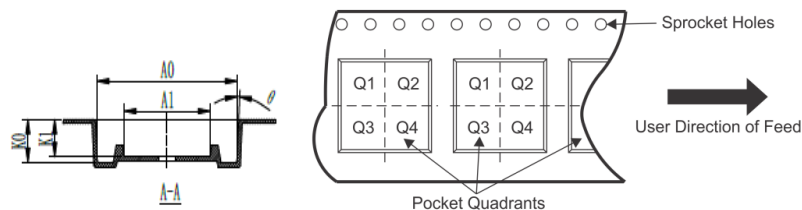
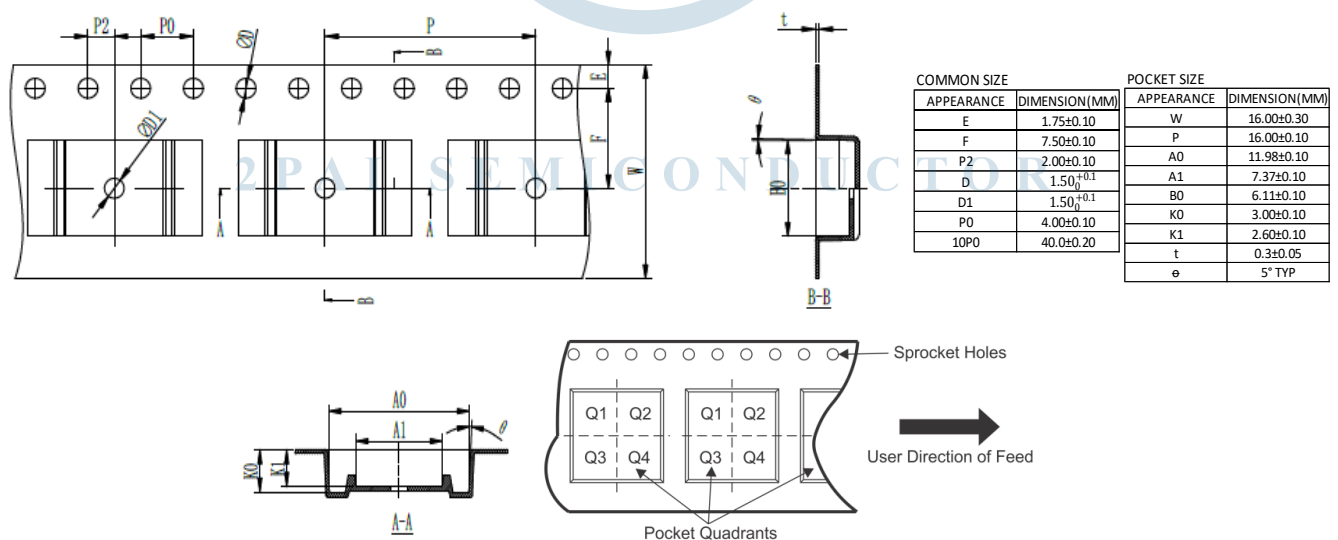
8-Lead Narrow Body SOIC [NB SOIC-8]



Note: The pin1 of the chip is in the quadrant Q1

Figure33. 8-Lead Narrow Body SOIC [NB SOIC-8] Reel Information—Dimension Unit(mm)

8-Lead Wide Body SOIC [WB SOIC-8]



Note: The pin1 of the chip is in the quadrant Q1

Figure34. 8-Lead Wide Body SOIC [WB SOIC-8] Reel Information—Dimension Unit(mm)

Top Marking



Line 1	Pai82XXX = Product name
Line 2	YY = Work Year WW = Work Week ZZ = Manufacturing code from assembly house
Line 3	XXXXX, no special meaning

Figure 35. Top Marking

ORDERING GUIDE

Table18. Ordering Guide

Model Name	Temperature Range	UVLO (V)	Output Current (A)	Isolation Rating (kVrms)	AEC-Q100	Package	MSL Peak Temp ⁽¹⁾	MOQ/ Quantity per reel ⁽²⁾
Pai8211A-SR	-40 to 125°C	8	6	3.75	NO	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211AQ-SR	-40 to 125°C	8	6	3.75	YES	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211C-SR	-40 to 125°C	12	6	3.75	NO	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211CQ-SR	-40 to 125°C	12	6	3.75	YES	NB SOIC-8	Level-2-260C-1 YEAR	4000
Pai8211A-W5R	-40 to 125°C	8	6	5.00	NO	WB SOIC-8	Level-2-260C-1 YEAR	1000
Pai8211AQ-W5R	-40 to 125°C	8	6	5.00	YES	WB SOIC-8	Level-2-260C-1 YEAR	1000
Pai8211C-W5R	-40 to 125°C	12	6	5.00	NO	WB SOIC-8	Level-2-260C-1 YEAR	1000
Pai8211CQ-W5R	-40 to 125°C	12	6	5.00	YES	WB SOIC-8	Level-2-260C-1 YEAR	1000

⁽¹⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽²⁾ MOQ, minimum ordering quantity.

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REVISION HISTORY

Revision	Date	Page	Change Record
1.0	2021/08/12	All	Initial version
1.1	2022/07/20	All	Change MSL from level 3 to level 2. Change regulatory information. Add Pai8211C and WB SOIC-8 package information.



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